PrimeYield

Fastest Pre-silicon Design Yield Analysis and Optimization

Overview

The Synopsys PrimeYield tool is the industry's fastest pre-silicon design yield analysis solution enabled by patented fast statistical methods and accelerated with breakthrough machine learning technology.

It delivers design yield analysis and optimization 100X-1000X faster than existing solutions and is scalable to volume production system-on-chips (SoCs) with billions of transistors, enabling SoC designers to shift-left design yield optimization to pre-silicon design phases.

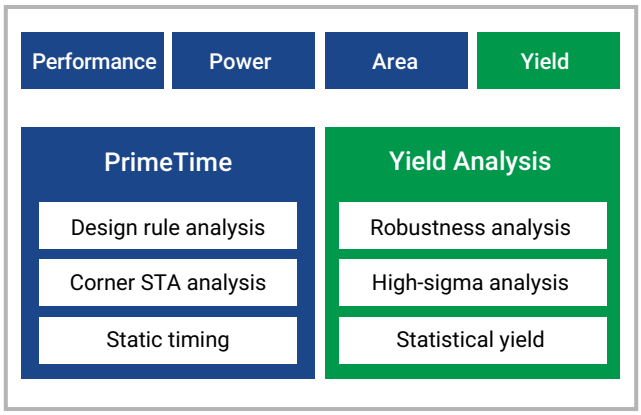

Figure 1: PrimeYield design yield analysis features

PrimeYield Capabilities

The PrimeYield innovative fast statistical engine uniquely leverages the core engines of the industry's gold-standard PrimeTime® signoff and HSPICE® simulation tools. It overcomes the turnaround time challenges that previously prohibited full statistical pre-silicon yield analysis with machine learning technologies, enabling pre-silicon design yield analysis and optimization for every design of any size.

With the addition of yield as a fourth design quality metric, now PPAY (power, performance, area, and yield), the Fusion Design Platform™ can deliver silicon designs that are faster, lower power and more cost effective.

Accelerated by machine learning technology, the PrimeYield solution performs fast Monte Carlo statistical simulation on critical timing paths with HSPICE accuracy within minutes, versus days or weeks required by full statistical simulations. Its patented parametric yield analysis with statistical correlation modeling enables statistical-based yield analysis and optimization on large-scale SoCs with billions of cells, an analysis previously feasible only for a few dozen cells.

PrimeYield can rapidly identify and drive optimization of yield-impacting cells caused by statistical correlation and sensitivity to various design variations, such as supply voltage drops or manufacturing variability, while using industry standard inputs for immediate deployment.

Features:

Full-chip parametric yield analysis

Parametric design timing yield analysis based on Monte Carlo statistical simulation identifies yield hotspots for yield optimization of large-scale SoC

Design yield robustness analysis

Identify and drive optimization of yield-impacting cells caused by process, voltage, and additional design variations

Critical path simulation

Fast Monte Carlo statistical path simulation that delivers true-HSPICE accuracy within minutes, including high-sigma accuracy support